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# TECHNIQUES TO ENABLE TIME OF DAY LOADING IN PLUGGABLE OPTICS BASED ON OBTAINING A 1PPS SIGNAL UTILIZING A REPURPOSED PIN FOR AN OPTICAL CONNECTOR

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## ABSTRACT

Obtaining a 1 Pulse Per Second (1PPS) signal is essential for delivering latency and jitter sensitive applications over a packet network through pluggable optics based on a disaggregated solution that may be applicable to service provider (SP) routing and/or server products for various applications. Techniques are presented herein that enable a 1PPS signal to be provided from a network router to an enhanced Small Form Factor Pluggable (SFP+) device by re-purposing an existing pin of an SFP+ connector for the SFP+ device.

## DETAILED DESCRIPTION

In a disaggregated architecture, application specific functionality can be handled through modular pluggable and re-programmable optics utilizing Small Form Factor Pluggable (SFP+) devices/modules. Typically, an SFP+ device/module is connected to a generic router/server platform in a Multi-Source Agreement (MSA) compliant SFP+ 20-pin connection to provide application functionality for a port, as prescribed by the Small Form Factor (SFF) Specification 8431.

Various applications can be delivered via the SFP+ form factor, such as Common Public Radio Interface (CPRI) over Radio over Ethernet (ROE), Private Line Emulation (PLE) for Optical Network Transport (OTN), Synchronous Optical Networking (SONET), Fibre channel and 10 Gigabit (10G) Ethernet over a packetized network, 10G Network Interface Device (NID), 10G Optical Network Unit (ONU), etc. The applications have stringent jitter and latency requirements and may present different technical challenges for addressing Packet Delay Variation (PDV) issues, enable phase/time/clock synchronization, variable delay that may be incurred due to buffering, retiming, and/or mapping/de-mapping

of different applications over an Ethernet link, all of which may result in asymmetrical delay issues.

It is necessary for smart pluggable devices to compensate for such latency and delay problems by staying synchronized with a network router by supporting ToD/1PPS operations.

For example, in some instances, it is necessary to support Time of Day (ToD) loading within a Smart SFP+ module for PDV compensation and re-timing constant bitrate (CBR) data over a 20 kilometer (km) fronthaul network. Consider an example involving CPRI over Ethernet in which CPRI, a commonly used front haul technology, requires a 8.138 nanosecond (nsec) one-way jitter, a Round Trip Time (RTT) jitter requirement of  $\pm 16.276$  nsec (e.g.,  $1/614$  megabits per second (mbps) = 16.276 nsec as per CPRI Specification Version 7 (v7)). Cloud or Centralized Radio Access Network (C-RAN) applications such as network Multiple-Input Multiple-Output (MIMO) have a transmit diversity (TX-DIVERSITY) requirement of  $\pm 32.5$  nsec and inter-band Carrier Aggregation (CA) or inter-band Cubic Metric (CM) Time Alignment Error (TAE) should be  $\pm 130$  nsec.

For CPRI, it is essential to have proper ToD support in a pluggable module (in order to meet end-to-end air interface alignment requirements) in which the pluggable module is also performing mapping, de-mapping, inserting PDV, and re-timing, along with enabling end-to-end phase and time synchronization to meet these requirements.

In order to support end-to-end CPRI communications over an Ethernet transport in fronthaul network, an approach with joint processing of the Ethernet packets carrying the CPRI bit stream with packet buffering and retiming of the packets at the receive end is used to meet the stringent timing and jitter requirements and essentially the PDV induced in the Ethernet network is cleaned through de-jittering.

In this approach, a maximum possible delay compensation time is used which is long enough to cover all possible jitter, fiber propagation delay, processing delay, serialization delay etc. The packet at the receive end is delay compensated by this maximum delay minus the time the packet took in reaching the received end. In this manner, all the CPRI traffic in the form of Ethernet frames is played out after the same maximum

possible delay compensation after adjusting for the transmit time and the PDV it incurred in the Ethernet transport path.

In order to enable the PDV cleaning and re-timing of the original data, it is required that the both ends which are performing CBR to packet mapping and the reverse links have the same ToD view without which, such strict requirements cannot be met. Therefore, there is a need for ToD counter support for the Smart SFP+ form factor that is aligned with a network router device timer such that the counter is to be continuously ticking with the network clock.

In another example, for passive optical network (PON) applications, due to the significant upstream delay caused by upstream scheduling and asymmetric bandwidth allocations in PON, the end-to-end point-to-point (PTP) over PON will not work. The PON protocol [ONU and Optical Line Termination (OLT)] involves a specific mechanism for transmitting the ToD details that cannot be communicate a PON endpoint obtains a proper ToD from a host. Thus, ToD is needed for an OLT pluggable module that is to distribute the ToD to an ONU and recovered at other end. Having ToD at the host alone is not sufficient.

In the case of CPRI or enhanced CPRI (eCPRI) in a Layer-3 (L3) based Ethernet network, ToD is needed to apply delay correction for handling the asymmetry between forward and backward paths. ToD is also needed in pluggable modules for meeting timing error requirements for class C timing. In short, many applications that may be deployed via a pluggable form factor may have stricter PDV cleaning, time/phase sync related requirements and may add more variable delays or latencies than an Ethernet PHY.

The network clock (SyncE) for the Smart SFP+ form factor is extracted from the system interface (XFI) of the SFP+ Transmitter Data In and Inverted Transmitter Data (TD+/TD-) pins, which is used for ticking the ToD counter. The 80-bit ToD data is transferred to an SFP+ module in the form of special Ethernet packets through the XFI interface from a host to the SFP+ module. Table 1, below, illustrates an SFP+ connector pinout definition.

**TABLE 1: SFP+ CONNECTOR PINOUT**

Pin Num.	PIN Name	Function
1, 20	VeeT	Transmitter Ground
2	TX Fault	Transmitter Fault Indication
3	TX Disable	Transmitter Disable
4	MOD-DEF2	A 2-wire serial interface, bidirectional data line
5	MOD-DEF1	A 2-wire serial interface, clock line
6	MoD-DEF0	Module absent, pulled low to indicate module is present
7	RATE SEL1	Select between full or reduced receiver bandwidth
8	LOS	Receiver loss-of-signal indication
9	RATE SEL0	Select between full or reduced transmitter bandwidth
10, 11, 14	VeeR	Receiver Ground
12	RD-	Inverted Receiver Data Output
13	RD+	Non-Inverted Receiver Data Output
15	VccR	Receiver Power
16	VccT	Transmitter Power
17	VeeT	Transmitter Ground
18	TD+	Transmit Data In
19	TD-	Inverted Transmitter Data In

During operation, the SFP+ module extracts the ToD data from the Ethernet packet and loads the ToD to the ToD counter maintained within the SFP+ module. The ToD loading is to occur at a time reference, which requires a 1PPS signal from the host. The rising edge of the 1PPS signal represents a second's boundary and is used for frequency correction. The SFP+ ToD has to be very closely synchronized with the network router, which creates a requirement for providing the 1PPS signal to the SFP+ module. The ToD loading from the network router to an SFP+ module occurs at a frequency of once for every one second and the seconds value of the ToD counter is updated every time at the edge of the 1PPS signal. The fixed delay inside an SFP+ module has to be compensated internally.

For Smart SFP+ modules that are to be compliant with an MSA, interoperability is to be ensured with all other MSA networking devices. To achieve such interoperability, such Smart SFP+ modules have to respect the standard SFP+ pinout as defined in Table 1.

As per the MSA agreement, there is no spare or reserved pin in an SFP+ connector that can be used to connect a 1PPS signal from a network router.

However, techniques herein enable a 1PPS signal to be provided from a network router to an SFP+ module by re-purposing an existing pin of the SFP+ connector.

Smart SFP+ modules that implement functionality for emulation engines are to carry timestamp information over Ethernet packets that is utilized at a remote end for generating a PTP ToD in an SFP+ Passive Optical Network (PON) Optical Line Terminal (OLT) for transferring the ToD/Phase using the PON protocol as per International Telecommunication Union Telecommunication (ITU-T) standards. This includes re-timing the data (cleaning up the PDV) for radio burst alignment on the air interface and measuring the network path delay to compensate the asymmetry delay.

For techniques herein, it is assumed that source and sink nodes have the same primary reference clock (PRC) and are synchronized to same start time. In order for a Smart SFP+ module to be synchronized to the same reference clock as its network node and start time, it needs a synchronous Ethernet (SyncE) clock, ToD, and a 1PPS signal. As shown in Figure 1, the clock recovered by the Smart SFP+ module from the System receive interface (TD+/TD-) is the network router clock and its SyncE accurate clock, which is used to tick ToD counter logic.

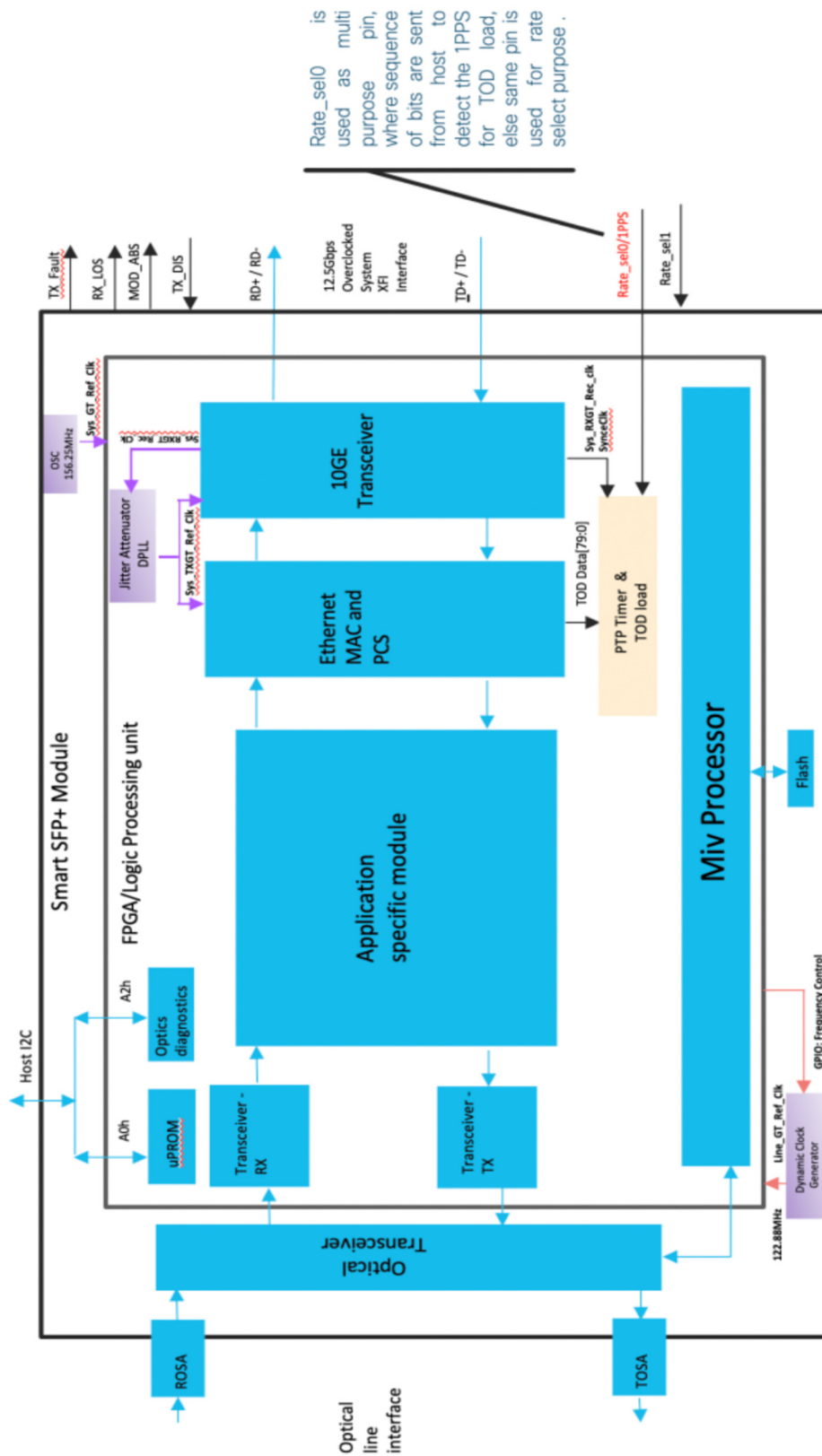


Figure 1: Smart SFP+ TOD Load Representation

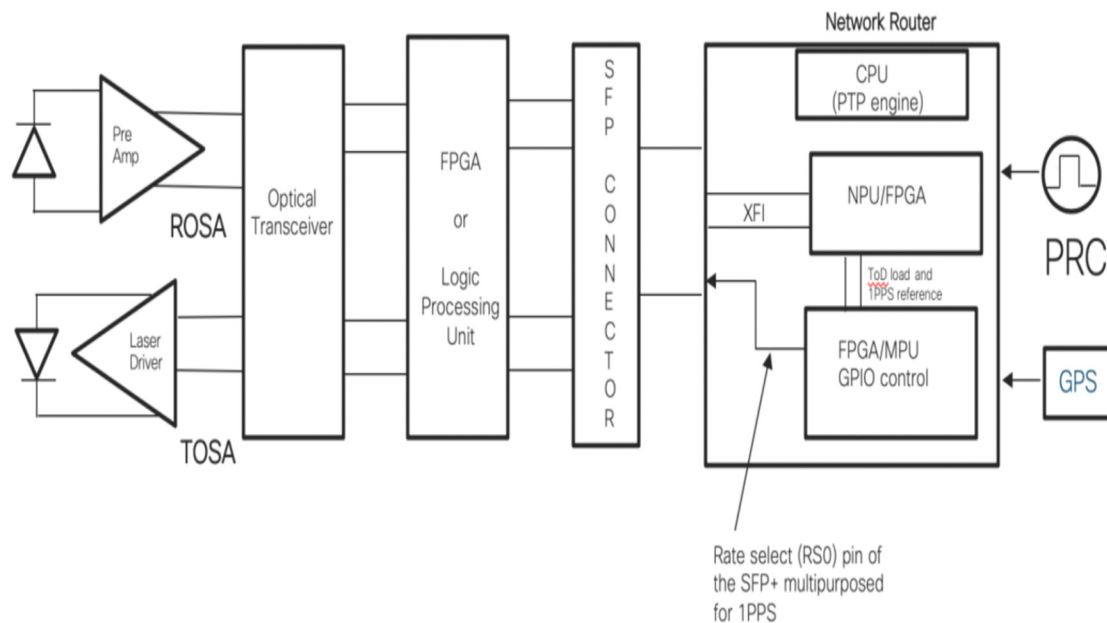
The ToD is periodically sent to the SFP+ module as shown in Figure 1 from a network router for every one second over specialized Ethernet packets. Ethernet Media Access Control (MAC) logic within the SFP+ module extracts the ToD data from the Ethernet packets and this data is loaded to the seconds' portion of the ToD counter. This is referred to as a ToD load in which the ToD load is to occur at the positive edge of the 1PPS signal.

As clearly illustrated from Table 1, above, since there is no existing pin available for the 1PPS signal and also as there is no reserved or free pins available on the SFP+ connector, as part of the techniques of the solution provided herein, it is proposed that the Rate Select 0 (RS0) pin can be utilized as a multipurpose pin for obtaining the 1PPS signal.

As illustrated in Figure 1, pins 7 and 9 of the SFP+ connector (RS0 and RS1, respectively) are the rate-select pins that control rate-select functionality. These pins are defined in SFF 8431 as logic high for bit rates greater than 4.25 Gigabits per second (Gbps) and logic low for 4.25 Gbps and below. RS1 is designated for the transmit (TX) and RS0 is designated for the receive (RX) in which the RS0 is provided a static signal that is driven by the network router.

In order to utilize the RS0 pin as a multipurpose pin for obtaining a 1PPS signal, logic present in the network router to drive the 1PPS signal is to be updated in order to generate the 1PPS indication to the Smart SFP+ module via the RS0 pin. Figure 2, below, illustrates example details of a 1PPS connection between a network router and SFP+ connector in which the RS0 pin of the SFP+ connector is utilized to obtain the 1PPS signal. A Field Programmable Gate Array (FPGA) or microprocessor (MPU)/Microcontroller in the network router can be used to control and multipurpose the RS0 pin in order to provide the 1PPS signal.





*Figure 2: Representation of Smart SFP+ Module Interconnected with a Network Router for a 1PPS Connection*

The network router may provide a 1PPS signal to pluggable optics utilizing one of two methods, which may include:

- The network router logic generating a positive pulse over the RS0 bit, which will be detected by the SFP+ as a 1PPS edge in order to load the ToD received from an Ethernet packet into the ToD load counter; or
- The network router logic generating a sequence of bits over the RS0 connection in which the sequence consists of 8 bits (8b1100\_0011) at a frequency of 125 Megahertz (MHz) to indicate the occurrence of the 1PPS edge to the Smart SFP+ module

The Smart SFP+ FPGA or logic processing unit may decode the 1PPS pulse or sequence and update its ToD counter with the already received ToD data from network router via the system interface. Only the seconds' values are loaded into the higher 48 bits of the ToD counter. The Smart SFP+ FPGA or logic processing unit is also responsible for ticking the nanosecond value (i.e., the lower 32 bits of the ToD counter) at the granularity of 8 nanoseconds (e.g., using a 125 MHz clock derived from the system

recovered clock). The network router has to ensure that it sends the ToD data via an Ethernet packet to SFP+ module before sending the 1PPS indication sequence via the RS0 pin of the smart SFP+ connector.

Thus, techniques herein may provide for the ability to create a new optics module that may be specifically focused on Fifth Generation (5G) fronthaul, midhaul, and backhaul (xHaul) transport networks. The techniques herein may enable end-to-end delivery of Layer 1 applications via the SFP+ pluggable form factor in which such applications may include CPRI (utilizing Institute of Electrical and Electronics Engineers (IEEE) 1914.3 RoE); enhanced CPRI (eCPRI); Low-PHY for 5G fronthaul, PON (ONU and OLT); Metro Ethernet Forum (MEF) 63 (MEF63) standards-based applications (e.g., 10G Physical Coding Sublayer (PCS), SONET (OC48, OC192) and/or OTU2 Clear Channel PLE, OTU2 Channelized (OTU2 <-> 8xODU0) PLE; Time Division Multiplexing such as TDM2IP; 10G NID features; IP security (IPSec); Network Function Virtualization accelerator; and interference engine support; among others. In short, smart SFP+ can be enabled with different applications, depending on use case, that may be required to support ToD/1PPS signaling within a pluggable form factor in order to synchronize timing with a network router.

In summary, techniques herein may enable a 1PPS signal to be provided from a network router to an enhanced SFP+ module by re-purposing an existing pin of the SFP+ connector. Enabling a 1PPS signal to be obtained by an SFP+ module is essential for delivering latency and jitter sensitive applications over a packet network. Such a pluggable optic disaggregated solution as provided by the techniques herein may be utilized by any combination of routing, switching, and/or server products as well as many applications. Additionally, the cost of a pluggable optic device that may be provided utilizing the techniques herein may provide a less expensive alternative to vendor and/or host-based solutions.